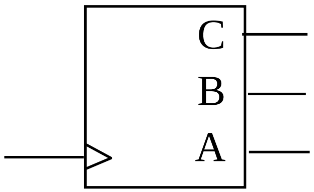
SEQUENTIAL CIRCUITS - III

DESIGN METHOD FOR SYNCHRONOUS COUNTERS

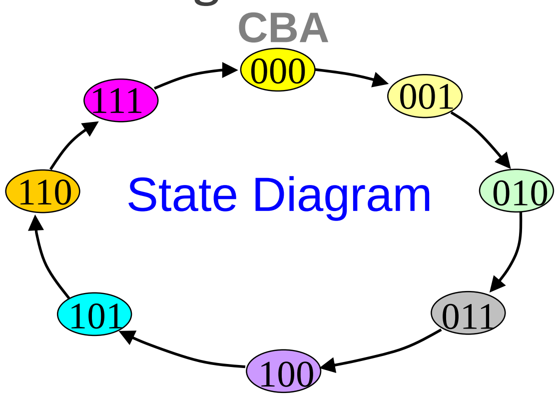
Design Method - Synchronous Counters

Goal : Given the state diagram of a counter realize it using common FFs (and combinational logic).

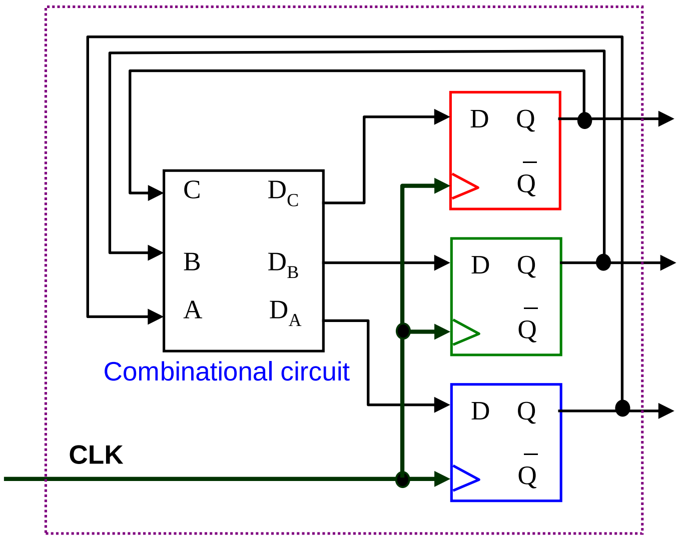
Example : **Design a *3-bit counter* having the following state diagram. Use D FFs.**



Functional block diagram of 3-bit counter.



3-bit synchronous counter



FF outputs are **fed back** to combinational circuit inputs.

Combinational circuit outputs D_A, D_B, & D_C are connected to D FF inputs and will be transferred to the output at next active clock edge.

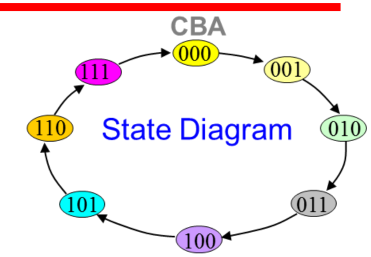
Key: Design combinational circuit to **take previous counter outputs** & **produce the next state**.

Systematic design method is similar to that used for FF conversion considered before.

Design Method : Steps

Step 1

- Draw a State Diagram for the desired Count Sequence

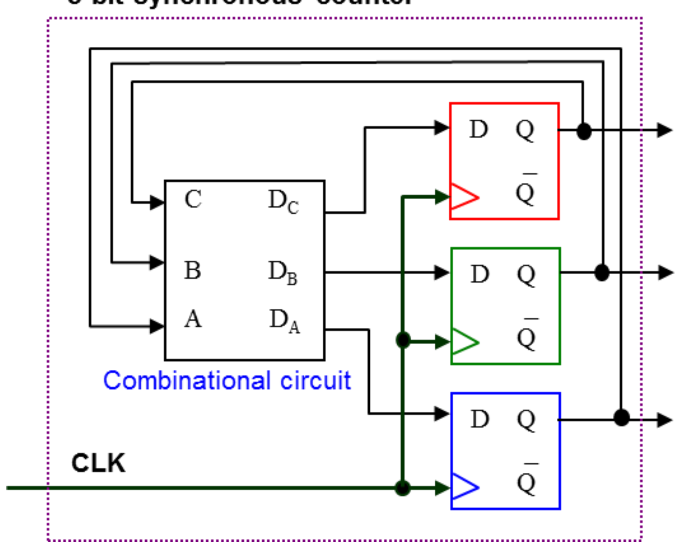


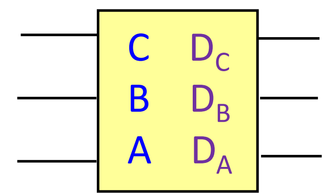
Step 2

- Determine the Functional Block Diagram of the N-bit Counter.

1) Number of flip-flops?
2) Inputs and Outputs of combinational circuit?

3-bit synchronous counter





Combinational Circuit

Inputs: Present-state counter outputs (A,B,C).

Outputs: Next-state counter outputs to connect to FF inputs. (D_A, D_B, D_C)

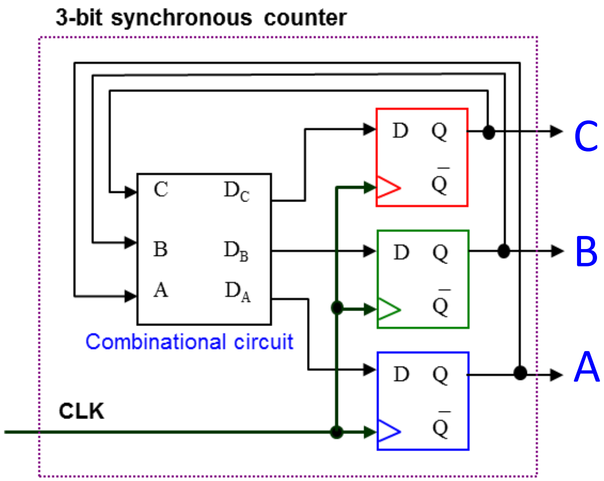
Design Method – Cont'd

Step 3A

- **Truth table of the combinational circuit.**
  A. Determine **next state table** for the counter.

Present-state outputs			Next-state outputs		
C	B	A	C^+	B^+	A^+
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	0

Next-State Table



A synchronous counter can be realized with D FFs or with any other FF

Design Method – Cont'd

***Excitation Table :** Specifies what the **FF** inputs should be for a specific Q $\rightarrow$ Q^+ transition to occur.

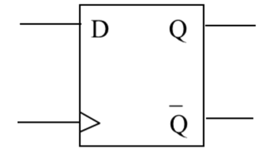
Step 3B

- **Truth table of the combinational circuit.**
  B. Using the excitation table, determine the output values of the combinational circuit.

Present-state outputs | Next-state outputs | Required FF input

C	B	A	C^+	B^+	A^+	D_C	D_B	D_A
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	0
0	1	0	0	1	1	0	1	1
0	1	1	1	0	0	1	0	0
1	0	0	1	0	1	1	0	1
1	0	1	1	1	0	1	1	0
1	1	0	1	1	1	1	1	1
1	1	1	0	0	0	0	0	0

Next-State Table

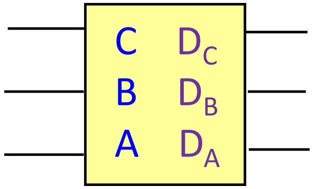


D Flip Flop Excitation Table

Q	Q^+	D
0	0	0
0	1	1
1	0	0
1	1	1

D $\Leftrightarrow$ Q^+

We now have a truth table for the combinational circuit!



Design Method – Cont'd

Step 4

- **Realize the circuit.**

Present-state outputs			Required FF input		
C	B	A	D_C	D_B	D_A
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	0

BA \ C	0	1
00	0	1
01	0	1
11	1	0
10	0	1

$$D_C = AB\overline{C} + \overline{B}C + \overline{A}C$$

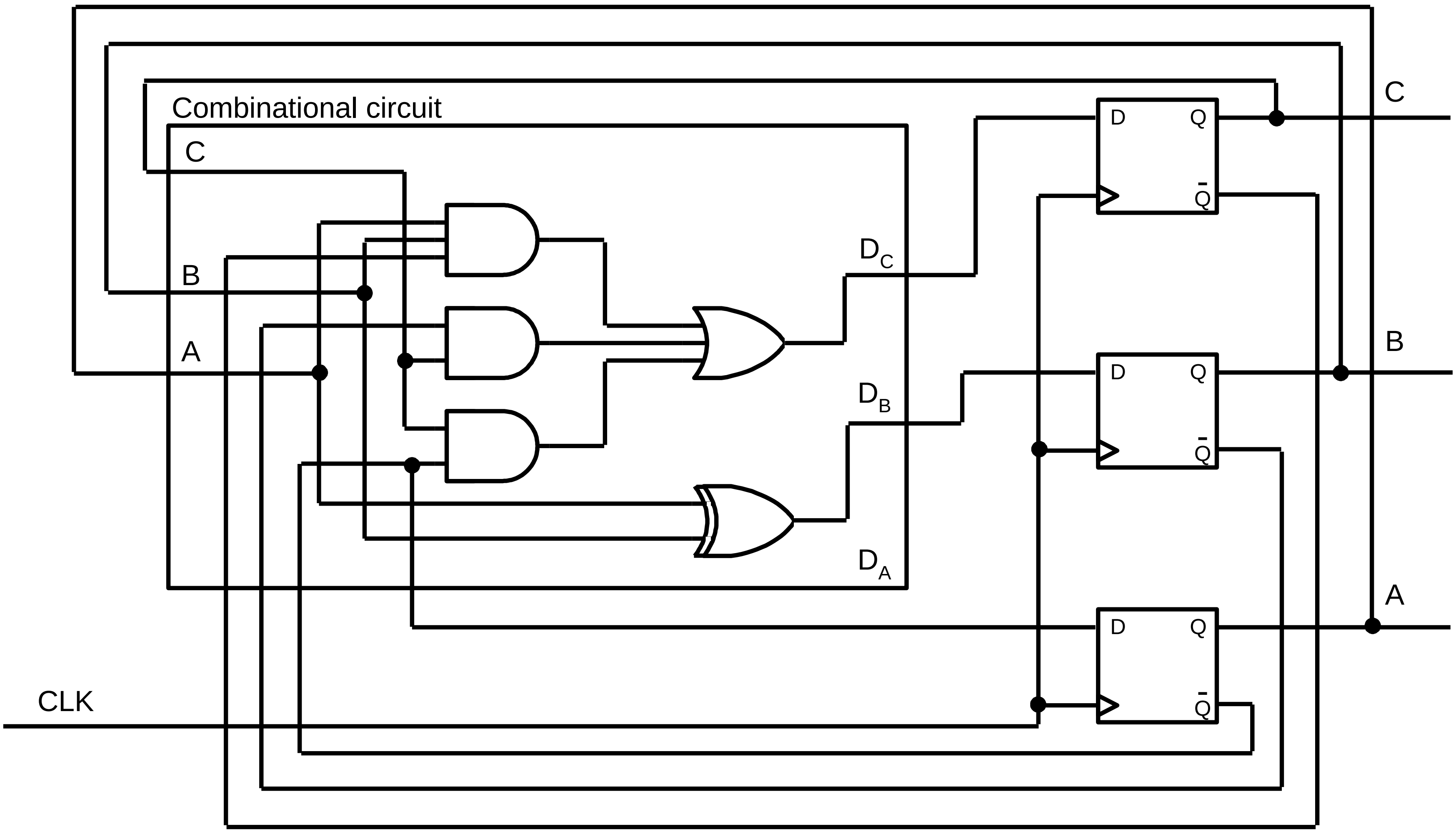
BA \ C	0	1
00	0	0
01	1	1
11	0	0
10	1	1

$$D_B = A\overline{B} + \overline{A}B = A \oplus B$$

BA \ C	0	1
00	1	1
01	0	0
11	0	0
10	1	1

$$D_A = \overline{A}$$

Synchronous 3-bit counter



Synchronous Counter Example 2

Design a synchronous counter with count sequence using DFFs:

101,001,000,010,110,100,101,… **(mod-6).**

The counter also has an external active high synchronous CLEAR input which will clear the counter to 000 at next active clock edge when set to ‘1’.

e.g. 101,001,000,010,110,100,000,010..

1) State Diagram

2) Functional Block Diagram

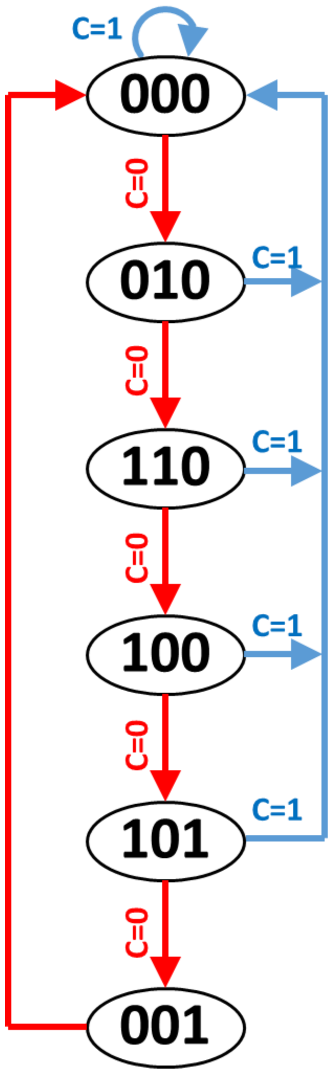
3) Next State Table / Truth table of C.C.

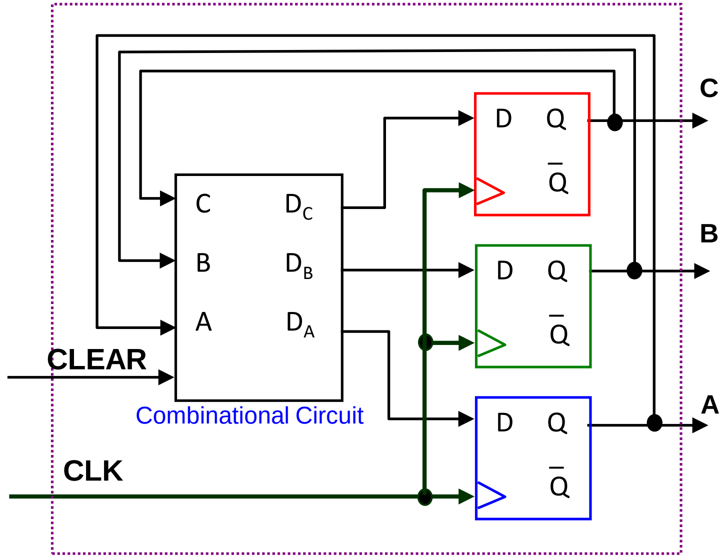
4) Final Implementation

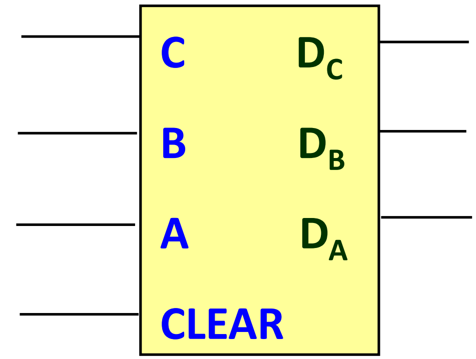
Step1: Write state diagram.

Step2: Determine functional block diagram of counter.

Step3 : Functional block diagram of combinational circuit.







Step4 : Get TT of combinational circuit using FF excitation table.

Step5 : Realize circuit.

CLEAR	C	B	A	C^+	B^+	A^+	D_C	D_B	D_A
0	0	0	0	0	1	0	0	1	0
0	0	0	1	0	0	0	0	0	0
0	0	1	0	1	1	0	1	1	0
0	0	1	1	X	X	X	X	X	X
0	1	0	0	1	0	1	1	0	1
0	1	0	1	0	0	1	0	0	1
0	1	1	0	1	0	0	1	0	0
0	1	1	1	X	X	X	X	X	X
1	X	X	X	0	0	0	0	0	0

SOP for flip-flop inputs

$$D_C = \overline{CLEAR} \bullet B + \overline{CLEAR} \bullet C \bullet \overline{A}$$

$$D_B = \overline{CLEAR} \bullet \overline{C} \bullet \overline{A}$$

$$D_A = \overline{CLEAR} \bullet C \bullet \overline{B}$$